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| **Screenshot** | **Signals Included** | **Description / Observation** |
| RESET\_Wave.png | reset | Reset signal goes high at 0ns, initializing all registers (like PC, ALU inputs, RegisterFile) to 0. Shows proper system initialization. |
| ALU\_Wave.png | ALU\_Result, Reg[1], Reg[2] | ALU\_Result signal shows correct operation (addition/subtraction) based on input registers Reg[1] and Reg[2]. Confirms ALU module functionality. |
| Clock\_wave.png | clk | Clock toggles at correct frequency, driving all sequential elements like Program Counter and registers. Ensures timing is proper across modules. |